08-11-00

A

Attorney Docket No.: CYPR-PM00005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.			
Express Mail Label No.:	EK381944575US	Name of Person Making the Deposit:	ANTHONY CHOU
Date of Deposit:	08/09/00	Signature of the Person Making the Deposit:	Anthony Chou

Inventor(s): Krishnaswamy Ramkumar, Kaichiu Wong and Venuka Jayatilaka

Title: PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Transmittal of a Patent Application
(Under 37 CFR §1.53)

Transmitted herewith is the above identified patent application, including:

- X Specification, claims and abstract, totaling 20 pages.
- ____ Formal drawings, totaling ____ pages.
- X Informal drawings, totaling 9 pages.
- X Declaration and Power of Attorney.
- X Information Disclosure statement.
- X Form 1449
- X Assignment(s)
- X Assignment Recordation Form (duplicate)
- ____ Preliminary Amendment
- ____ Other: ____

FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. § 1.16 and for recording of the Assignment, if any, are determined as follows:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$690.00
Total Claims	29	Minus 20=	9	X $18 =	$162.00
Independent Claims	4	Minus 3=	1	X $78=	$78.00
If multiple dependent claims are presented, add $260.00					$0.00
Add Assignment Recording Fee of $40.00 If Assignment document is enclosed					$40.00
TOTAL APPLICATION FEE DUE					$970.00

rev. 11/98 wmh

PAYMENT OF FEES

The full fee due in connection with this communication is provided as follows:

1. Not enclosed

   [ ] No filing fee is to be paid at this time.

2. Enclosed

   [X] Filing fee

   [X] Recording assignment

   [ ] Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached

   [ ] For processing an application with specification in a non-English language

   [ ] Processing and retention fee

   [ ] Fee for international-type search report

   [X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

   [X] A check in the amount of $970.00

   [ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

This application is filed pursuant to 37 C.F.R. § 1.53 in the name of the above-identified Inventor(s).

Please direct all correspondence concerning the above-identified application to the following address:

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[X] This transmittal ends with this page.

Respectfully submitted,

Date: 8/9/2000

By: _____
Anthony C. Murabito
Reg. No. 35,295

UNITED STATES PATENT APPLICATION FOR

PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

Inventors:

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PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor processing. More specifically, the present invention relates to the isolation of active areas on a semiconductor wafer.

RELATED ART

Isolating adjacent active areas is a very essential requirement as device dimensions are scaled down on an integrated circuit (IC). As the scaling gets down below 0.25 um technology, the Local Oxidation of Silicon (LOCOS) isolation scheme fails because the thickness of the grown isolating oxide is not adequate for the narrow space. In addition, the large encroachment associated with the LOCOS scheme makes it difficult to get the required active area width. LOCOS also has high temperature and long oxidation periods. Shallow Trench Isolation (STI) is widely used to isolate active areas in VLSI technologies with critical dimensions less than 0.25 um. This method provides robust isolation when the space between P+ and N+ active areas gets down below about 0.80 um since the thickness of the isolation regions is not significantly limited and the encroachment is very small.

The STI process used currently involves creation of trenches of depth of about 3000 angstroms to 4000 angstroms in silicon in regions where isolation spaces are to be formed. The pattern of the spaces is etched in a silicon nitride layer deposited on top of a pad oxide. After the formation of the trench pattern, silicon dioxide is deposited by a Chemical Vapor Deposition (CVD) process to fill the trenches. The oxide is polished using the silicon nitride as the stopping layer. The nitride is then stripped off to get the pattern of the active areas with isolating oxide spaces.

Shallow Trench Isolation however, has its own problems nominally because the oxide in the isolating regions is not grown but deposited and the stress levels in this oxide can become very high. The stress levels may be increased further by the shape of the active/isolation pattern. Active areas with sharp bends or corners are more prone to problems with stress. This stress, combined with the damage caused by plasma etch such as spacer etch lead to the formation of nucleation sites for dislocations. Bombardment by heavy ions such as arsenic during ion implantation can lead to dislocations in the silicon crystal in these sites. These dislocations at the surface when intersecting the source/drain to substrate P-N junctions can give rise to severe reverse leakage in these junctions that can either seriously affect the functionality of a Static Random Access Memory (SRAM) cell or can give rise to very high standby current in the cell.

Stress induced defects are seen near poly lines. When a poly line crosses an active area, there is likely to be a gouge into the active area next to the poly edge due to the poly/spacer etch. The gouge may also generate some nucleation sites for dislocations. The extent of gouge and or dislocation generation is decided by the quality of the oxide at the edge of the active area, which is mainly the liner oxide. Depending on where the poly line intersects the active area, the extent of damage caused by the spacer etch may be different. When the active area is straight, the liner oxide grown after trench etch is stress free and hence may be able to withstand the poly/spacer etch better. On the other hand, when the active area has a corner, the liner oxide grown in this region has high stress and hence may be more prone to gouge when a poly line crosses the corner. Thus in a SRAM cell, a poly line crossing the corner of an active area may give rise to dislocations. This will lead to leakage in the N+ to P-substrate junctions which will lead to failure of the cell.

SUMMARY OF THE INVENTION

Accordingly, what is needed is a method and process for the fabrication of an isolation region in a semiconductor which will reduce or eliminate leakage between active areas. What is needed yet is a method and process in which the fabrication time for an isolation region in a semiconductor is reduced. What is also needed is a method and process which allows the further shrinkage of integrated circuits to smaller sizes compatible with the next technology generation. The present invention provides these advantages and others not specifically mentioned above but described in the sections to follow.

A method and process are disclosed for the fabrication of an isolation region in a semiconductor crystal. The method and process may be used in the fabrication of isolation regions used for the separation of adjacent active areas in an integrated circuit. A shallow trench is created on the surface of the semiconductor in regions where isolation spaces are to be formed. A layer of silicon dioxide (LINOX) is then grown over the surfaces of the trench. The LINOX covers roughened regions formed along the surfaces of the trench during its formation.

In one embodiment of the present invention, the liner oxidation recipe calls for growing the LINOX in the presence of oxygen and chlorine at a temperature of about 1000 degrees Centigrade. In one embodiment of the present invention, immediately following the growth of the LINOX, the

temperature is increased to about 1050 degrees Centigrade for a period of time sufficient in order to anneal the LINOX. The remaining volume of the trench is then filled with silicon dioxide by Chemical Vapor Deposition (CVD). The surface of the semiconductor is then polished to reveal the pattern of active areas with isolating oxide regions.

In one embodiment of the present invention, the step of annealing the LINOX provides a number of distinct advantages. First of all, annealing greatly reduces stresses in the LINOX and in the surrounding semiconductor material. Annealing also increases the density of the LINOX. Thus annealing increases the LINOX resistance to damage or gouge during any subsequent etching; for instance during a poly/spacer etch. This leads to a reduction in dislocations in the semiconductor crystal and an attendant reduction in electrical leakage around the isolation region. In one embodiment of the present invention, the electrical leakage in a SRAM cell with shallow trench isolated active areas having sharp corners is reduced. A more robust LINOX and a reduction in electrical leakage around an isolation region allows for the further shrinkage of integrated circuit dimensions. In one embodiment of the present invention, a reduction in the dimensions of a Static Random Access Memory (SRAM) cell is made possible. Furthermore, denuding and gettering of the semiconductor are both accomplished during the annealing step which results in a shortening of total processing time. Finally, since gouging of the LINOX no longer occurs

where poly/spacer etch overlaps an active area corner, restrictions on the placement of poly lines have been eliminated.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an exemplary Shallow Trench Isolation scheme in accordance with one embodiment of the present invention.

Figure 2 is the cross-sectional view of a single trench in accordance with one embodiment of the present invention.

Figure 3 illustrates a cross-sectional view showing the grown Liner Oxide (LINOX) applied to the walls of the trench, in accordance with one embodiment of the present invention.

Figure 4 illustrates a cross-sectional view showing silicon dioxide trench filler deposited by Chemical Vapor Deposition (CVD) in accordance with one embodiment of the present invention.

Figure 5 is a process diagram of the recipe for annealing the LINOX in accordance with one embodiment of the present invention.

Figure 6 is a cross-sectional view showing a poly line passing over a Shallow Trench Isolation (STI) region in accordance with one embodiment of the present invention.

Figure 7 illustrates a cross-sectional view showing possible damage after Poly/spacer etch in accordance with one embodiment of the present invention.

Figure 8 illustrates a planar-view showing Poly/spacer edge overlapping an active area corner in accordance with one embodiment of the present invention.

Figure 9 illustrates a cross-sectional view showing the minimal Poly/spacer etch damage after annealing the LINOX in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, a process for reducing leakage in a SRAM cell with shallow trench isolated active areas, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail, as not to unnecessarily obscure aspects of the present invention. For instance, the substrate used could be silicon or could also be other substrate materials, such as SiGe.

Figure 1 illustrates an exemplary Shallow Trench Isolation (STI) scheme in accordance with one embodiment of the present invention. An integrated circuit may be realized by locating active semiconductor devices in the active regions 110, 120 and 130. Electrical isolation of active regions may be realized by the formation of shallow trenches in the surface of the semiconductor substrate between the active regions, which may then be filled with silicon dioxide to form isolation regions 140. The minimization or elimination of electrical leakage currents between active regions along a leakage path 150 is a primary objective. In the present invention, the process used to form isolation regions 140 results in a reduction in electrical leakage currents between active regions when compared with prior art methods. These and other advantages of

the present invention not specifically enumerated above will become clear within discussions of the present invention below.

Figure 2 is the cross-sectional view of a shallow trench 210 separating two active regions 220 and 230 in a semiconductor substrate 200 in accordance with one embodiment of the present invention. In one embodiment of the present invention, the trench may be formed by plasma etching. A small trench width 250 may be preferred to accommodate smaller integrated circuit geometry. A larger trench depth 260 may reduce electrical current leakage between active regions 220 and 230. The plasma etch used to form the trench results in uneven trench surfaces 240. These uneven surfaces lead to the formation of stress regions and dislocations in the active regions during subsequent processing steps as described below. Regions of stress and dislocations may in turn result in increased electrical leakage between active areas as well as active device failure. In one embodiment, the shallow trench having a width of at most 0.3 μ with fallback widths of 0.25 μ and 0.21μ.

In the present invention, a layer of silicon dioxide, referred to as the Liner Oxide layer (LINOX) , may be grown over the inner surfaces of the trench to cover the unevenness and to reduce occurrences of dislocations. Figure 3 illustrates a cross-sectional view 300 showing the grown Liner Oxide (LINOX) 330 covering the uneven inner surfaces of the trench 340. The trench separates the two active regions 310 and 320. Since the LINOX 330 is grown, it

becomes an integral part of the semiconductor substrate, as opposed to silicon dioxide that is deposited on the surface of the substrate by Chemical Vapor Deposition (CVD). Following the LINOX growth step, the temperature is elevated slightly for a period of time to anneal the LINOX 330. In one embodiment of the present invention, the LINOX 330 may be grown at a temperature of 1000 degrees centigrade, and annealing of the LINOX 330 may be accomplished over a period of 3 hours at a temperature of 1050 degrees centigrade.

Annealing causes an increase in density of the LINOX 330 which increases its strength and relieves stresses which may form along the trench surfaces at corners or at sharp edges. The increased strength of the LINOX 330 causes it to be insensitive to subsequent processing steps. Relieving the stresses in the LINOX 330 (especially at the corners) may result in a reduction in or elimination of dislocations in the semiconductor substrate which in turn may reduce electrical leakage currents between active areas. An additional advantage of the present invention is the accomplishment of denuding and gettering that occur during the annealing process.

Figure 4 illustrates a cross-sectional view 400 of a Shallow Trench Isolation (STI) region 450 separating two active regions 410 and 420. The silicon dioxide trench filler 430 may be deposited by Chemical Vapor Deposition (CVD) in accordance with one embodiment of the present invention.

The LINOX 440 separates the deposited CVD oxide 430 from the semiconductor substrate active regions 410 and 420. As a result, the large stresses that occur when oxide is deposited by CVD directly into a trench without the LINOX may be eliminated. Thus the dislocations formed in the semiconductor substrate due to these stresses may also be eliminated in accordance with the present invention.

Figure 5 is an exemplary process diagram 500 which may be used to grow a liner oxide (LINOX) in a shallow trench on a semiconductor substrate in accordance with one embodiment of the present invention. At step 510, the semiconductor temperature is stabilized in the presence of Argon at 1000 degrees centigrade. In step 520, the LINOX is grown to the desired depth by holding the semiconductor at a temperature of 1000 degrees centigrade in the presence of oxygen and chlorine for a period of time. The semiconductor temperature is then increased in step 530 to 1050 degrees centigrade for a period of three hours to accomplish the annealing of the LINOX. During step 530, the density of the LINOX is increased density, stresses between the LINOX and the semiconductor substrate are relieved, and denuding and gettering are both accomplished. In step 540, the temperature is then reduced to the starting point of 800 degrees centigrade for further processing. It is appreciated that other possible gases besides Argon can be used, and also other possible sources of oxygen can be used.

In subsequent processing steps, appropriate electrical connections between components to form an integrated circuit can be made by utilizing polysilicon (poly) strips as conductors. As illustrated in the cross-sectional view 600 in Figure 6, the poly 610 may pass over both active regions 650 as well as isolation regions 620 and 630. Etching of the poly, during a step referred to as poly/spacer etch, may gouge the liner oxide 640 at points of excessive stress 660.

In the present invention, the density of the liner oxide is greatly increased by annealing which reduces or eliminates gouging. Figure 7 is a cross-sectional view 700 illustrating regions where dislocations 710 may occur when the liner oxide 750 is not annealed. The combination of stress and gouging in the liner oxide 750 may cause dislocations 710 in the active regions 740 of the semiconductor substrate as illustrated in Figure 7. Such dislocations may increase electrical current leakage around isolation regions 720 and 730, and may result in active device failures. Such gouging and dislocation formation are particularly troublesome when a poly/spacer edge overlaps an active area at a sharp corner.

Figure 8 illustrates a planar-view 800 of a semiconductor wafer. Two active regions 810 are separated by a shallow trench isolation region 820. An etched poly line 830 overlaps a sharp corner of the upper active region 810. The gouge region 840 is an area where possible gouging and dislocations may

occur as a result of the poly/spacer etch. In the present invention, annealing of the LINOX in the trench 820 reduces or eliminates gouging during poly/spacer etch. As a result, dislocations are eliminated which reduces electrical current leakage between active regions. Furthermore, limitations on the layout of poly lines are relaxed since annealing the LINOX has eliminated the gouging problem.

Figure 9 is the cross-sectional view 900 of an active area 930 separated by two isolation regions 910 and 920 in which the LINOX 940 has been annealed in accordance with one embodiment of the present invention. Annealing of the LINOX has increased the density of the LINOX, reduced the stresses between the LINOX and the semiconductor active area. The gouging and resultant dislocations that may occur at points 950 during poly/spacer etch have been eliminated. As a result, the problems caused by poly/spacer etch over active areas with sharp corners no longer exist. Thus, prior limitations placed on the topology of poly lines have been eliminated.

The preferred embodiment of the present invention, a process for reducing leakage in a SRAM cell with shallow trench isolated active areas, is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is Claimed is:

1. A method of forming an isolation region in a semiconductor substrate comprising the steps of:

a) annealing a liner oxide in a trench in the surface of said semiconductor substrate, and

b) backfilling said trench with a bulk oxide.

2. The method according to Claim 1 wherein said semiconductor substrate comprises silicon.

3. The method according to Claim 1 wherein said liner oxide comprises silicon dioxide.

4. The method according to Claim 1 wherein said bulk oxide of said step b) comprises silicon dioxide.

5. The method according to Claim 1 wherein said annealing step further denudes and getters at least one of said substrate and said liner oxide.

6. The method according to Claim 1 wherein said annealing step reduces stresses in said liner oxide.

7. The method according to Claim 1 wherein said annealing step reduces the number of dislocations in said semiconductor.

8. The method according to Claim 1 further comprising the step of etching a trench in the surface of said semiconductor substrate and wherein said step of etching is done using plasma etching said semiconductor substrate to form said trench.

9. The method according to Claim 1 wherein said step b) is done using chemical vapor deposition.

10. The method according to Claim 1 wherein said annealing step further reduces the leakage between active regions in said semiconductor substrate.

11. A process for reducing leakage in forming an integrated circuit, structure comprising the steps of;

a) annealing a liner oxide layer in a shallow trench within a semiconductor substrate under conditions sufficient to reduce the rate of dislocations within said integrated circuit; and

b) chemical vapor depositing an oxide in said shallow trench.

12. A process as described in Claim 11 further comprising the steps of:

using a plasma etching process to form said shallow trench within said semiconductor substrate; and

growing a liner oxide layer over the surfaces of said shallow trench.

13. A process as described in Claim 11 wherein said annealing step is performed to also increase the density of said liner oxide.

14. A process as described in Claim 11 wherein said substrate further comprises a layer containing polysilicon over said shallow trench, and said method further comprises the step of performing a polysilicon etch over said shallow trench.

15. A process as described in Claim 11 wherein said step a) is performed also to achieve gettering and denuding.

16. A process as described in Claim 11 wherein said shallow trench is no greater than approximately 0.3 microns wide.

17. The process according to Claim 11 wherein said semiconductor is silicon.

18. The process according to Claim 11 wherein said liner oxide is silicon dioxide.

19. The process according to Claim 11 wherein said oxide of said step d) is silicon dioxide.

20. The process according to Claim 11 wherein said annealing step reduces relieves stresses in said liner oxide.

21. The process according to Claim 11 wherein said annealing step allows the width of the trench to be smaller than that realized without said annealing step.

22. The process according to Claim 11 wherein said annealing further reduces the leakage between active regions in said semiconductor.

23. A process for forming the isolation regions in a semiconductor substrate comprising the steps of:

a) etching a trench in the surface of said semiconductor substrate, said trench having corners therein;

b) growing a liner oxide in said trench;

c) annealing said liner oxide to reduce stresses at said corners; and

d) backfilling said trench with a bulk oxide.

24. The process according to Claim 23 wherein said linear oxide is increased in density as a result of said steps c) and d).

25. The process according to Claim 23 wherein said step c) reduces the number of dislocations formed in said substrate.

27. A process for growing and annealing liner oxide (LINOX) in a trench formed on the surface of a semiconductor comprising;

a) growing said liner oxide in said trench at a first temperature, and

b) annealing said liner oxide at a second temperature higher than the first temperature elevated above that used in said step a) sufficient to reduce relieve stresses in said liner oxide.

28. The process according to Claim 27 wherein denuding and gettering are achieved in said semiconductor during annealing said liner oxide.

29. The process according to Claim 27 wherein the leakage between active regions in said semiconductor is improved.

PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT

WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

ABSTRACT OF THE INVENTION

A method and process reducing or eliminating electrical leakage between active areas in a semiconductor separated by isolation regions. A method and process are disclosed for the fabrication of an isolation region in a semiconductor. The method and process can be used in the fabrication of isolation regions used for the separation of adjacent active areas in an integrated circuit. A shallow trench is created on the surface of the semiconductor in regions where isolation spaces are to be formed. A layer of silicon dioxide (LINOX) is then grown over the surfaces of the trench. The LINOX covers roughened regions formed along the surfaces of the trench during its formation. The LINOX is then annealed at a temperature above the LINOX deposition temperature for a period of time. Annealing reduces stresses in the LINOX and in the surrounding semiconductor material. Annealing also increases the density of the LINOX. Thus annealing increases the LINOX resistance to gouge during subsequent processing. This leads to a reduction in dislocations in the semiconductor and a reduction in electrical leakage around the isolation region. A more robust LINOX and a reduction in electrical leakage around an isolation region allows the further shrinkage of integrated circuit dimensions. Furthermore, denuding and gettering of the semiconductor are both accomplished during the annealing step which results in a shortening of total processing time. Finally, since gouging of the LINOX no longer occurs where poly/spacer etch overlaps an active area corner, restrictions on placement of poly lines have been eliminated.

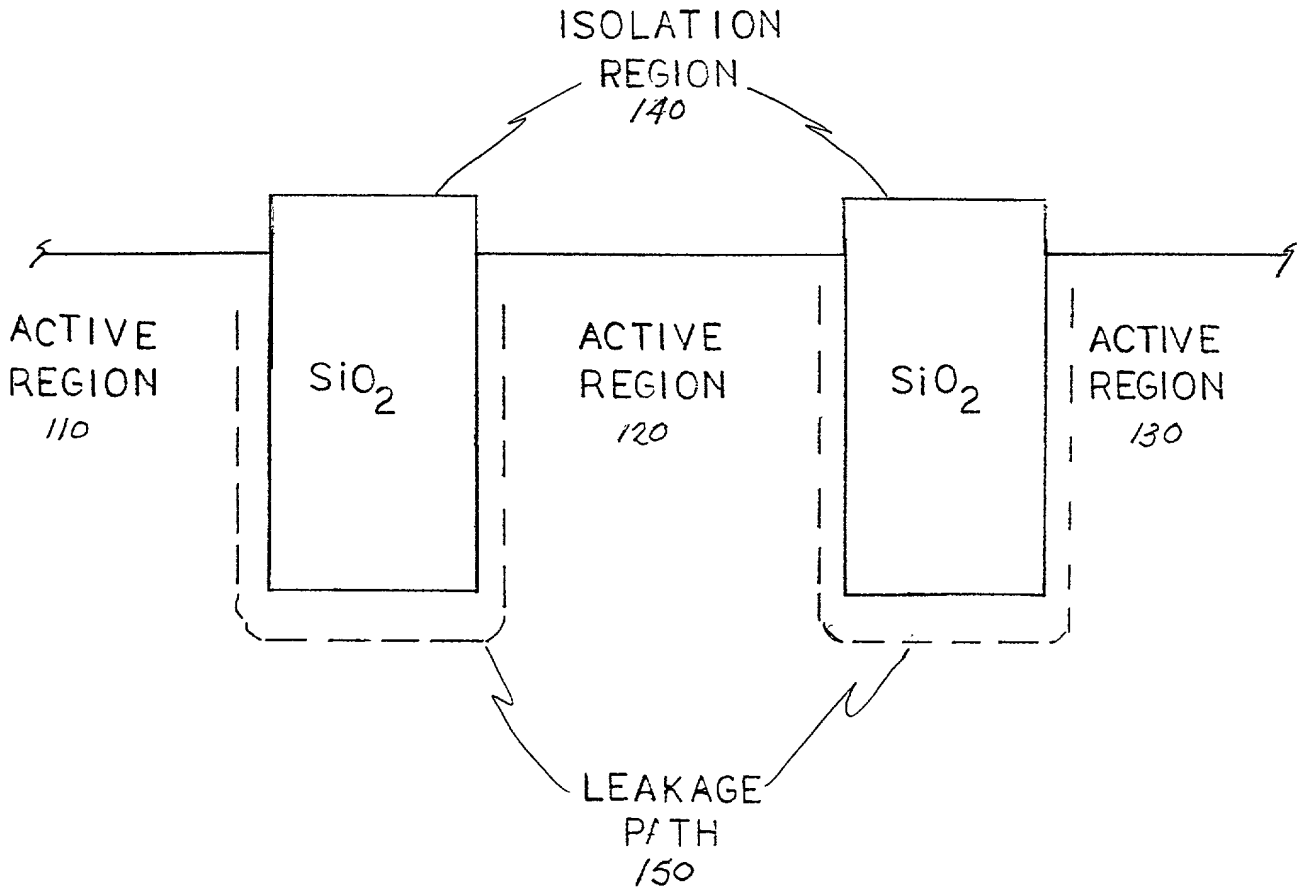
ISOLATION
REGION
140
ACTIVE
REGION
110
SiO2
ACTIVE
REGION
120
SiO2
ACTIVE
REGION
130
LEAKAGE
PATH
150

FIGURE 1

200

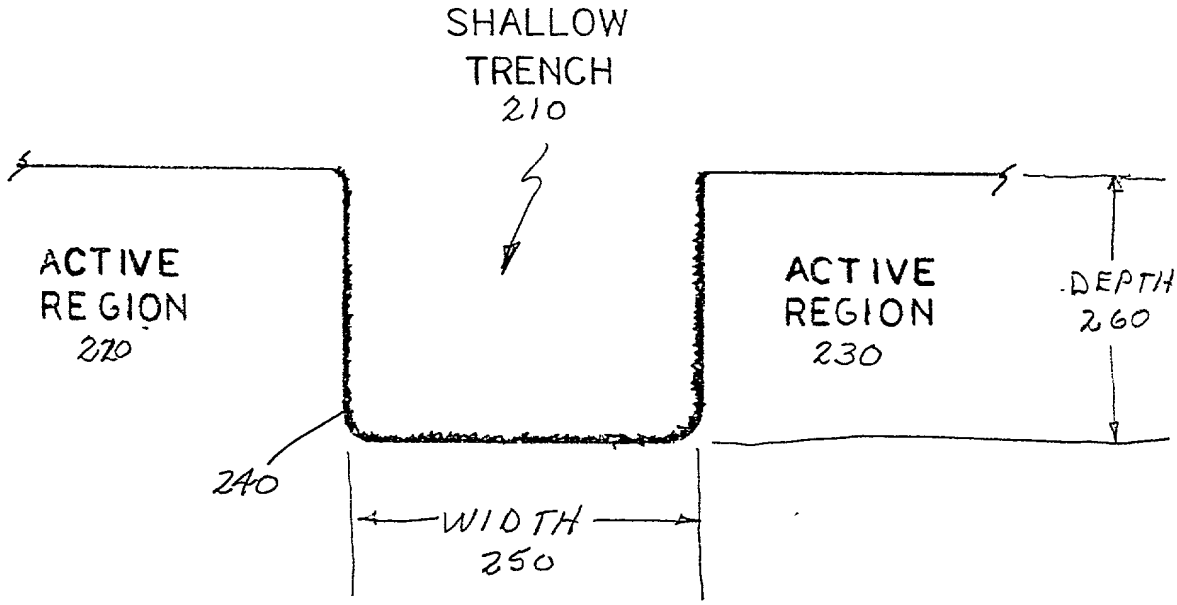
SHALLOW
TRENCH
210
ACTIVE
REGION
220
ACTIVE
REGION
230
DEPTH
260
240
WIDTH
250

FIGURE 2

300

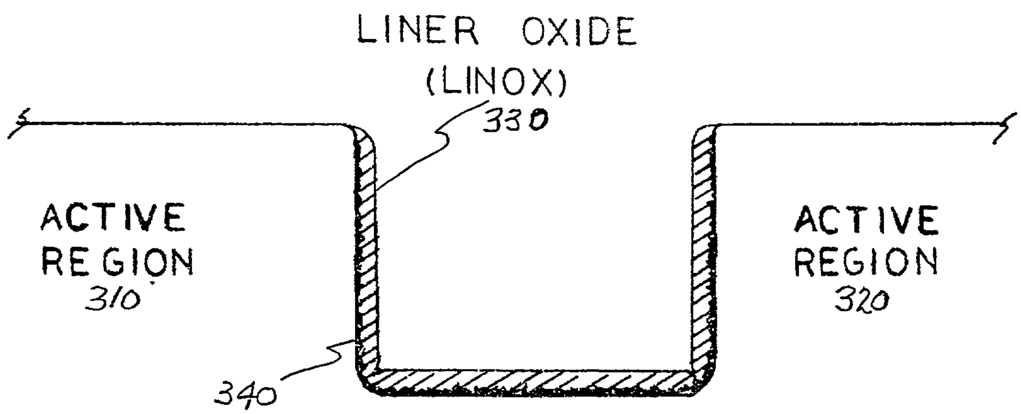

FIGURE 3

400

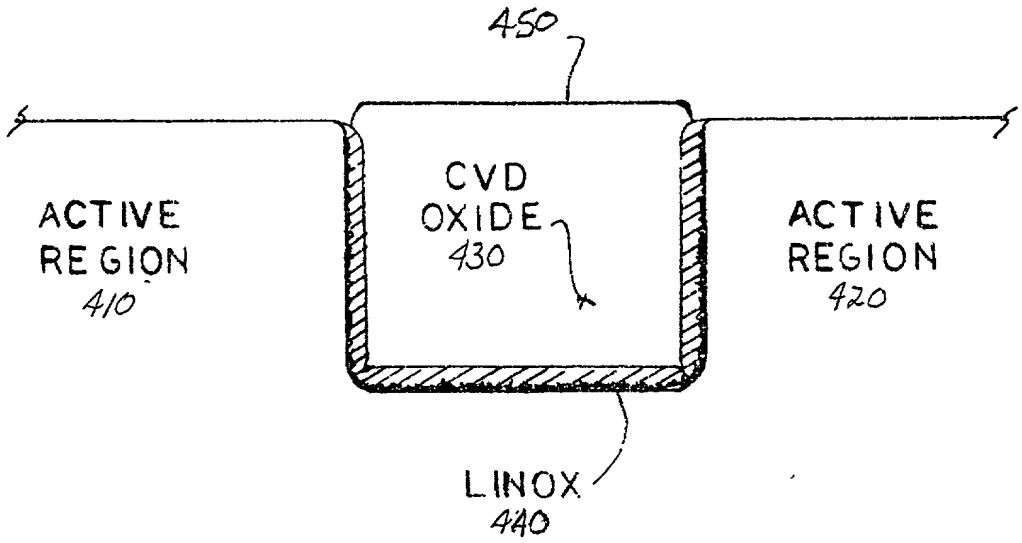
450
ACTIVE
REGION
410
CVD
OXIDE
430
ACTIVE
REGION
420
LINOX
440

FIGURE 4

500

Proposed Liner Oxidation recipe

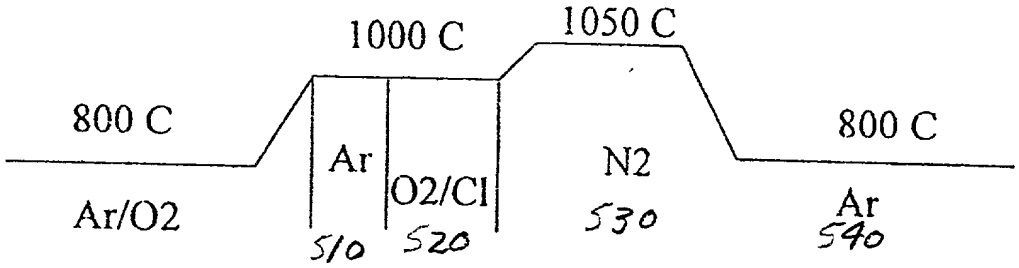

FIGURE 5

600

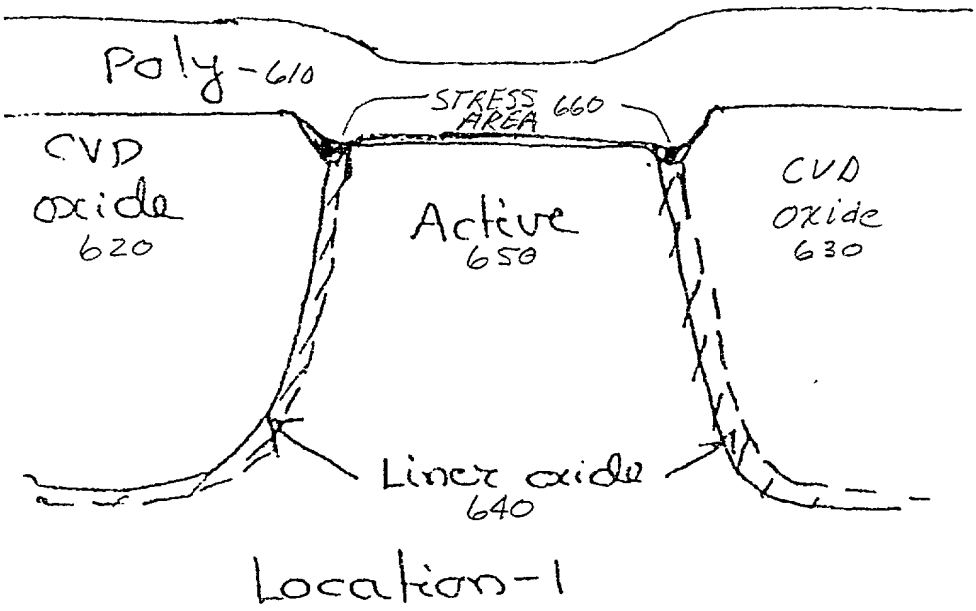
Poly - 610
STRESS AREA 660
CVD oxide 620
Active 650
CVD oxide 630
Liner oxide 640
Location-1

FIGURE 6

700

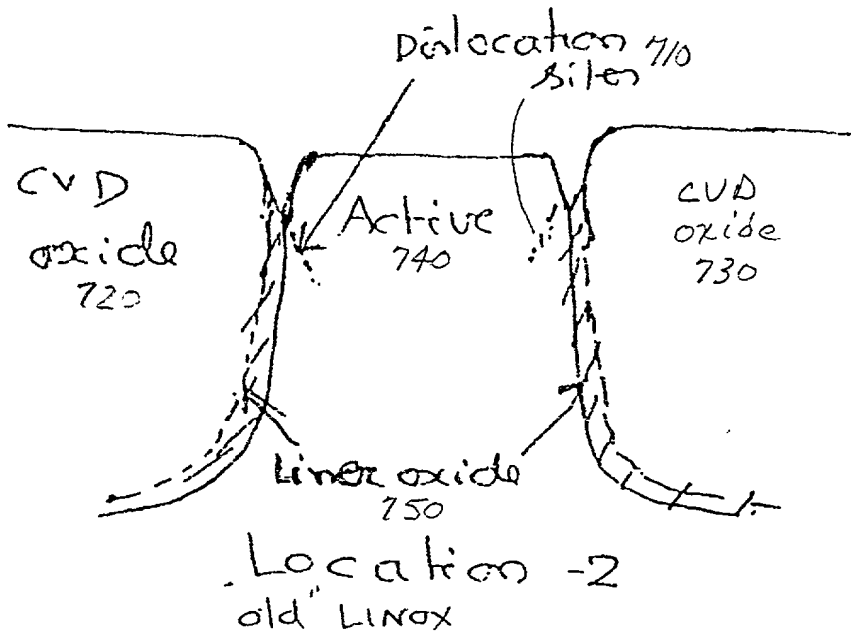
Dislocation sites 710
CVD oxide 720
Active 740
CVD oxide 730
Liner oxide 750
Location -2
old LINOX

FIGURE 7

800

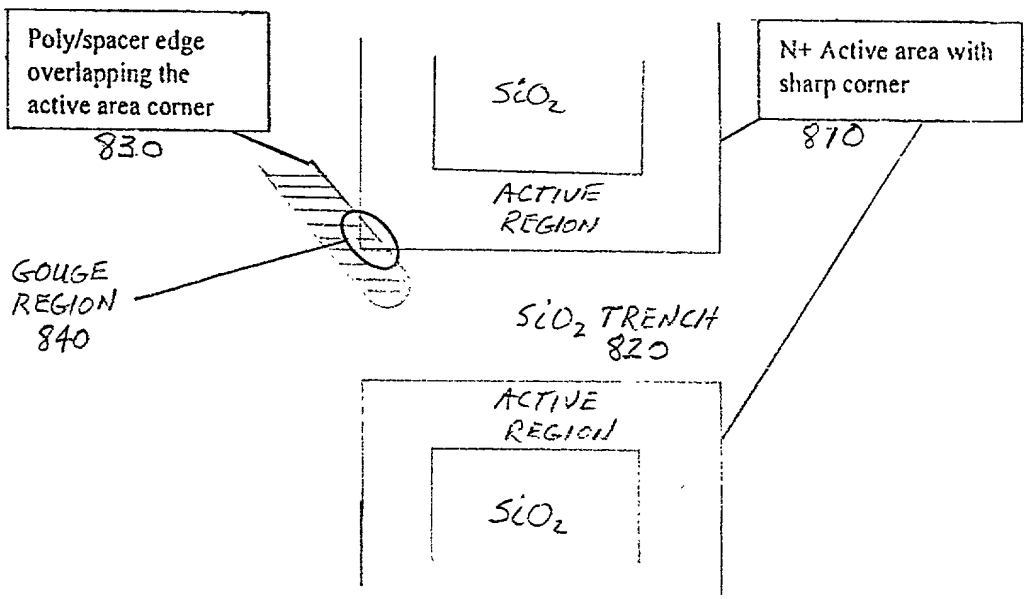
Poly/spacer edge overlapping the active area corner
830
N+ Active area with sharp corner
810
SiO_2
ACTIVE REGION
GOUGE REGION 840
SiO_2 TRENCH 820
ACTIVE REGION
SiO_2

FIGURE 8

900

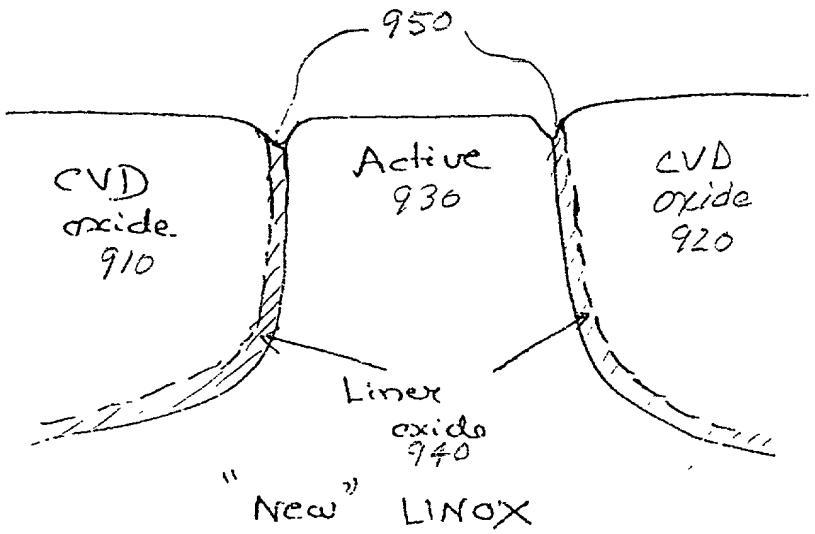
950
CVD
oxide
910
Active
930
CVD
oxide
920
Liner
oxide
940
"New" LINOX

FIGURE 9

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PROCESS FOR REDUCING LEAKAGE IN AN INTEGRATED CIRCUIT WITH SHALLOW TRENCH ISOLATED ACTIVE AREAS

the specification of which:

X is attached hereto, or
_____ was filed on _____ as application serial no. _____ : and
_____ was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed	
			_____ yes	_____ no
			_____ yes	_____ no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: 42,293
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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